CLAIMS

We Claim:

1. A delay locked loop comprising:

a primary delay line comprising a plurality of series-connected delay elements, wherein each of the delay elements has an adjustable delay;

a delay control circuit coupled to the primary delay line; and

at least one configuration memory cell coupled to the delay control circuit;

wherein the delay control circuit adjusts delay of the delay elements of the primary delay line in response to the at least one configuration memory cell.

2. The delay locked loop of Claim 1, further comprising:

a voltage distribution line, wherein each of the delay elements operates in response to a voltage on the voltage distribution line;

a first voltage terminal for receiving a first voltage; and

a second voltage terminal for receiving a second voltage, wherein the first voltage is greater than the second voltage;

wherein the delay control circuit selectively couples the first voltage terminal or the second voltage terminal to the voltage distribution line responsive to the at least one configuration memory cell.

3. The delay locked loop of Claim 2, wherein the first voltage terminal is coupled to the voltage distribution line when the at least one configuration memory cell stores a first data value, and wherein the second voltage terminal is coupled to the voltage distribution line when the at least one configuration memory cell stores a second data value.

4. The delay locked loop of Claim 2, wherein the first voltage is 10 or more percent greater than the second voltage.

5. The delay locked loop of Claim 2, wherein each of the delay elements comprises a plurality of series-connected inverters.

6. The delay locked loop of Claim 5, wherein each of the inverters comprises a p-channel transistor having a source coupled to the voltage distribution line.

7. The delay locked loop of Claim 5, wherein each of the inverters comprises a transistor having a well region coupled to the voltage distribution line.

8. The delay locked loop of Claim 2, wherein each of the delay elements exhibits a first delay when the voltage distribution line is coupled to receive the first voltage, and a second delay when the voltage distribution line is coupled to receive the second voltage, wherein the second delay is greater than the first delay.

9. The delay locked loop of Claim 8, wherein the second delay is about twice as long as the first delay.

10. The delay locked loop of Claim 2, further comprising:

a clock input terminal for receiving an input clock signal, wherein the clock input terminal is coupled to an input terminal of the primary delay line;

a first multiplexer coupled to receive delayed versions of the input clock signal from the delay elements of the primary delay line; and

a delay selection circuit coupled to control the first multiplexer in response to the input clock signal and a distributed version of the input clock signal.

11. The delay locked loop of Claim 10, further comprising:

a second multiplexer having a first input terminal coupled to receive a delayed version of the input clock signal routed by the first multiplexer; and

a fast delay element having an input terminal coupled to receive the delayed version of the input clock signal routed by the first multiplexer, and an output terminal coupled to a second input terminal of the second multiplexer.

12. The delay locked loop of Claim 11, wherein the delay selection circuit is coupled to control the second multiplexer.

13. The delay locked loop of Claim 11, wherein the fast delay element selectively provides one of a plurality of delays.

14. The delay locked loop of Claim 11, further comprising a clock distribution network coupled to an output terminal of the second multiplexer, wherein the distributed version of the input clock signal is provided at an end of the clock distribution network.

15. The delay locked loop of Claim 2, further comprising a voltage regulator for providing at least one of the first and second voltages.

16. A field programmable gate array (FPGA) comprising:

an input clock terminal for receiving an input clock signal used to clock data into the FPGA;

a global clock routing network that provides a distributed clock signal in response to the input clock signal, wherein the distributed clock signal is used to clock data into or out of the FPGA;

a delay locked loop that forces the distributed clock signal into a fixed phase relationship with the input clock signal by introducing signal delay to the input clock signal, wherein the delay locked loop includes:

a primary delay line comprising a plurality of series-connected delay elements, wherein each of the delay elements operates in response to a voltage on a voltage distribution line;

a first voltage terminal for receiving a first voltage;

a second voltage terminal for receiving a second voltage, wherein the first voltage is greater than the second voltage; and

a voltage selection circuit for selectively coupling the first voltage terminal or the second voltage terminal to the voltage distribution line.

17. The FPGA of Claim 16, wherein each of the delay elements comprises a plurality of series-connected inverters.

18. The delay locked loop of Claim 17, wherein each of the inverters comprises a p-channel transistor having a source coupled to the voltage distribution line.

19. The delay locked loop of Claim 17, wherein each of the inverters comprises a transistor having a well region coupled to the voltage distribution line.

20. A method of operating a delay locked loop comprising:

applying an input clock signal to a delay line including a plurality of series-connected delay elements, each of the delay elements having a voltage-controlled delay;

operating the delay elements in response to a first voltage when the input clock signal has a frequency greater than or equal to a first frequency; and

operating the delay elements in response to a second voltage when the input clock signal has a frequency less than the first frequency.

21. The method of Claim 20, further comprising:

programming a configuration memory cell to store a data value;

operating the delay elements in response to the first voltage when the data value has a first state; and

operating the delay elements in response to the second voltage when the data value has a second state.

22. The method of Claim 20, wherein the first voltage is greater than the second voltage

23. The method of Claim 22, wherein the first voltage is at least 10 percent greater than the second voltage.

24. The method of Claim 20, further comprising:

routing a delayed version of the input clock signal from a delay element of the primary delay line to a global clock routing network, whereby a distributed clock signal is provided at an end of the global clock routing network;

comparing the distributed clock signal with the input clock signal; and

selecting the delayed version of the input clock signal in response to the step of comparing the distributed clock signal with the input clock signal.

25. The method of Claim 24, the routing step further comprising:

routing a first delayed version of the input clock signal from a delay element of the primary delay line

to a fast delay element, wherein the fast delay element provides a second delayed version of the input clock signal; and

selectively routing either the first delayed version of the input clock signal or the second delayed version of the input clock signal to the global clock routing network, whereby the distributed clock signal is provided at an end of the global clock routing network.

26. The method of Claim 25, further comprising:

comparing the distributed clock signal with the input clock signal; and

selecting the first delayed version of the input clock signal or the second delayed version of the input clock signal in response to the step of comparing the distributed clock signal with the input clock signal.